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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,213	04/21/2004	Katsuyuki Kawamura	247322002200	9355

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EXAMINER	
GUPTA, PARUL H	
ART UNIT	**PAPER NUMBER**
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,213	KAWAMURA ET AL.	
	Examiner	Art Unit	
	Parul Gupta	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4 and 5* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 are pending for examination as interpreted by the examiner. The amendment and arguments filed on 4/6/07 were considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Suzu, US Patent 5,854,772. col. 3, lines 1-2

Regarding claim 1, Suzu discloses in figure 1 a decoder circuit (~~abstract~~) and mounted on an integrated circuit ("semiconductor memory device" of column 3, line ~~28~~), decoding an input voltage supplied to a single external input terminal into three or more control outputs (OUT A0-OUTA7), the decoder circuit comprising: a P-type transistor comprising an emitter (source) connected to a power source line of a high level (column 1, lines 29-31), a base (gate) connected to the external input terminal (column 1, lines 46-49) and a collector (drain) configured to be a first output terminal of a first control output (column 1, lines 31-33); and an N-type transistor comprising an emitter (source) connected to a power source line of a low level (ground as given in column 1, lines 44-45 is a power source of low level), a base (gate) connected to the external input terminal (column 1, lines 46-49) and a collector (drain) configured to be a second output terminal of a second control output (column 1, lines 36-39). Column 2, lines 50-53

explain that each circuit in figure 1 has the same configuration. Thus, 8 different control outputs are given in the configuration, where the p-channel transistor QA07 and the n-channel transistor QA16 is combined to obtain two separate outputs at the same time.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Kitayama, US Patent 5,418,762 in view of Suzu.

Regarding claims 4 and 5, Kitayama teaches in column 8, lines 12-47 an optical pickup including a photo-detecting amplifier circuit ("RF amplifier") for a disk recording/reproducing apparatus that uses a decoder circuit ("address decoder"). Kitayama does not but Suzu teaches an apparatus being capable of switch function by means of a decoder circuit (multiple outputs of figure 1), comprising: a decoder circuit comprising a P-type transistor and a N-type transistor and generating a first control output and second control output (shown in figure 1 as explained in the rejection of claim 1); and an amplifier (element used to select the output signal wire out of eight output signal wires as given in column 2. lines 50-53) receiving the first and second control outputs and generating signals (H or L); and an optical element responsive to one of the signals (H or L) generated by the amplifier (column 2, lines 26-41), wherein the P-type transistor comprises an emitter (source) connected to a power source line of

a high level (column 1, lines 29-31), a base (gate) connected to the external input terminal (column 1, lines 46-49) and a collector (drain) configured to be a first output terminal of a first control output (column 1, lines 31-33), and the N-type transistor comprises an emitter (source) connected to a power source line of a low level (ground as given in column 1, lines 44-45 is a power source of low level), a base (gate) connected to the external input terminal (column 1, lines 46-49) and a collector (drain) configured to be a second output terminal of a second control output (column 1, lines 36-39). Column 2, lines 50-53 explain that each circuit in figure 1 has the same configuration. Thus, 8 different control outputs are given in the configuration, where the p-channel transistor QA07 and the n-channel transistor QA16 is combined to obtain two separate outputs at the same time. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the decoder circuit as taught by Suzu into the system of Kitayama. The motivation would be to reduce the number of tranistor elements to minimize the size of the circuit (column 3, lines 14-20 of Suzu).

Allowable Subject Matter

4. Claims 2 and 3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The closest prior art is listed below, although the combinations would alter the functioning of the circuits.

Regarding claim 2, Suzu teaches the decoder circuit according to claim 1. Suzu does not but Arakawa teaches in figure 12 (explained further in column 16, lines 40-60) a circuit further comprising: one or more voltage decreasing means (Qg and Qh) of which one end (base) is connected to the external input terminal; and one or more first additional transistor in which a base (gate) is connected to the other end of the voltage decreasing means or to one of contacts of the voltage decreasing means, and an emitter (source) is connected to the power source line of high level or low level (Vpp/Vcc), and a collector (drain) is an output terminal of a control output (Vl).

Regarding claim 3, Suzu teaches the decoder circuit according to claim 1. Suzu does not but O'Shaughnessy teaches in figure 7B a circuit further comprising: a first voltage-dividing circuit (1041), standing between the external input terminal and the base (gate) of the P-type transistor (1044), in which four or more voltage-dividing resistors (only 3 shown, but number of resistors depends on resistance of each) are connected in series between the power source lines (VDD and VSS), the external input terminal is connected to a first contact of the voltage-dividing resistors (immediately after 1043), the base (gate) of the P-type transistor is connected via a bias resistor (inherent resistance in base of transistor) to a second contact of the voltage-dividing resistors (1043), and the base (gate) of the N-type transistor (1045) is connected via a bias resistor (inherent resistance in base of transistor) to a third contact of the voltage-dividing resistors (1042), the second contact having a voltage level higher than that of the first contact, the third contact having a voltage level (Vh) lower than the first contact (VSS) (voltages and relationships between contacts depend on the resistors and can be

controlled to yield this result); one or more first additional transistor (1050 and 1051) in which a base (gate) is connected via a bias resistor (inherent resistance in base of transistor) to a contact having a voltage level lower than the first contact (Although REX is given to be equivalent to VDS, the voltages of 1041 are controlled depending on the values of the resistors. Thus, the values of the resistors may be altered to yield this result.); a second voltage-dividing circuit (1042 to VDD) to which current taken in the P-type transistor (i_{Vh}) is supplied; and one or more second additional transistor (1046-1049) in which a base (gate) is connected via a bias resistor (inherent resistance in base of transistor) to a contact of voltage-dividing resistors of the second voltage-dividing circuit.

Response to Arguments

5. Applicant's arguments with respect to all claims have been considered but are not persuasive. The applicant contends that the decoder circuit of the claimed invention outputs at least two different control outputs while Suzu's circuit can output only one control output. However, column 2, lines 50-53 of Suzu explains that each circuit in figure 1 has the same configuration. Thus, 8 different control outputs are given in the configuration, where the p-channel transistor QA07 and the n-channel transistor QA16 can be combined to obtain two separate outputs at the same time.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parul Gupta whose telephone number is 571-272-5260. The examiner can normally be reached on Monday through Thursday, from 9:30 AM to 7 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PHG
5/23/07

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER